REMARKS

I. Introduction

In response to the pending Office Action, Applicants have amended the specification to include a reference to gate 34 illustrated in Fig. 4 so as address the objection to the drawings. In addition, claims 1-3, 4-8 and 10 have been amended so as to clarify the distinctions between the present invention over the cited prior art. Further, new claim 11 has been added. No new matters has been added.

Applicants note with appreciation the indication of allowable subject matter being recited by claims 2, 3, 7 and 8. Applicants and Applicants' attorney also wish to thank the Examiner for his time and courtesy during the interview conducted on April 14, 2004 during which there was a discussion regarding the differences between the present invention and the prior art references.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art references.

II. The Rejection Of The Claims Under 35 U.S.C. § 103

Claims 1, 4, 5, 6, 9 and 10 were rejected under 35 U.S.C. § 103 as being unpatentable over USP No. 5,938,774 to Hsu. For the following reasons, it is respectfully submitted that claims 1 and 4, as amended, are patentable over Hsu.

As recited by claims 1 and 6, the present invention relates to a circuit which allows for the correction of faulty memory locations. More specifically, the device comprises in-part a ***stored data selection section*** which operates to divide a given word of output data of the storage means and the correction data into a plurality of bytes, and selectively output in the same word, on a byte-by-byte basis, either an Mth byte (where M is an integer and $0 \leq M < 2^N$) of the divided

output data of the storage means or an Mth byte of the divided correction data. An exemplary circuit for implementing the stored data selection section 17 is shown in Fig. 2 of the specification. As shown therein, the 32 bit words from the SROM (i.e., storage means) and the SCDT (correction data) are each divided into four bytes in the byte selector 19, and the byte selector 19 allows bytes from either word to be output in the output word SDT under control of the byte selection controller 18.

As a result of the structure of the present invention, the circuit can advantageously provide a stored data modifier that can modify data starting at any arbitrary address on the storage medium. In contrast, as is the case with Hsu, the prior art systems require that the modified data start at an address which is a multiple of a 2^N address, or an access boundary as defined by the Applicants' specification.

Turning to the cited prior art, it respectfully submitted that, at a minimum, nowhere does Hsu disclose or suggest a circuit comprising any elements corresponding to the claimed stored data selection section of the present invention. First, referring to Figs. 2 and 3a-3c of Hsu, it is clear that Hsu does not disclose or suggest any structure that is capable of dividing a given word of either the output of the ROM 60 or the corrected data 70 into a plurality of bytes. Further, Hsu does not disclose or suggest any structure that would allow for one of the given the bytes of either the stored data in ROM 60 or the corrected data 70 to be output in the same data word. Indeed, as described by Hsu in col. 4, it appears that Hsu only provides for the output of either the data stored in ROM 60 or the corrected data 70. Nowhere does Hsu disclose that the ROM data and the corrected data can be output together in a given word.

Thus, as each and every limitation must be disclosed or suggested by the cited prior art reference in order to establish a *prima facie* case of obviousness (see, M.P.E.P. § 2143.03), and

at a minimum, Hsu fails to disclose or suggest the claimed stored data selection section for the reasons set forth above, it is respectfully submitted that claims 1 and 6 are patentable over Hsu.

III. All Dependent Claims Are Allowable Because The Independent Claims From Which They Depend Are Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, ***Hartness International Inc. v. Simplimatic Engineering Co.***, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as all independent claims are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also in condition for allowance.

IV. Conclusion

Accordingly, it is urged that the application is in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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